

1 REAL TIME DEBUGGER INTERFACE FOR EMBEDDED SYSTEMS

2
3 This application is a continuation of U.S. Serial No.
4 09/064,474, filed April 22, 1998, which is hereby incorporated by
5 reference herein in its entirety.
6

7 BACKGROUND OF THE INVENTION

8
9 1. Field of the Invention

10 The invention relates to systems and methods for debugging
11 software in real time. More particularly, the invention relates
12 to systems and methods for the real time debugging of firmware in
13 embedded systems, e.g. ASIC chips having one or more processors on
14 a single chip.
15

16 2. State of the Art

17 Software debugging may be accomplished in a number of ways,
18 some of which are not performed in real time. A traditional
19 debugging technique is to step through program instructions at a
20 rate much slower than the rate at which the program is designed to
21 run in real time. By stepping through the program instructions
22 one-by-one, errors can be observed as they happen and the program
23 code lines executed immediately prior to the error can be analyzed
24 to find the cause of the error. This technique is not helpful,

1 however, if the error in program execution is the result of timing
2 errors or other types of errors which only occur when the program
3 is running at real time speed. As used herein, the term "real
4 time" means the rate at which a program must execute in order to
5 process the incoming data rate which may be quite high.

6
7 A widely used technique for debugging a program which is
8 running in real time is called "tracing". Tracing involves
9 recording the transactions performed by the computer as it
10 executes the program code. The trace of activities performed by
11 the computer during the time of a failure can be a useful guide in
12 isolating possible causes of the failure.

13
14 Another useful debugging tool is to set breakpoints at
15 selected places in the program. The breakpoints trap the flow of
16 the software and provide insight into whether, when, and how
17 certain portions of the software are entered and exited. An
18 analysis of the flow of the software can provide information which
19 is useful in isolating bugs.

20
21 Many state-of-the-art tracing and trapping methods are
22 accomplished by a debug support circuit which is connected to the
23 system bus, i.e. the bus which couples the CPU to memory. See,
24 for example, U.S. Patent Number 5,491,793 to Somasundaram et al.

1 entitled "Debug Support in a Processor Chip." Connecting a debug
2 circuit to the system bus is convenient because addresses,
3 instructions, and data can be accessed via the system bus.
4 However, coupling the debug support circuit to the system bus
5 increases the electrical load on the bus and interferes with the
6 operation of the bus. Moreover, operation of the system bus may
7 interfere with operation of the debug support circuit. In
8 addition, the system bus may not provide all the information
9 necessary for debugging a program running on a CPU which uses
10 internal cache. These CPUs will not access the system bus if the
11 information they need is available in cache. If an error occurs
12 while the CPU is accessing internal cache, the debug support
13 circuit will not be able to access the information it needs.
14

15 Another tracing and trapping method is disclosed in U.S.
16 Patent Number 5,833,310 to Whistel et al. entitled "On-Chip In-
17 Circuit-Emulator Memory Mapping and Breakpoint Register Modules."
18 According to this method, an internal bus controller is coupled to
19 the memory address bus and a match register. When a memory
20 address written to the address bus matches an address in the match
21 register, a memory mapping module maps a memory cycle to an
22 external debug memory. The user can set specific bus event
23 conditions for which memory is mapped by writing to a set of
24 breakpoint registers. A disadvantage of this method is that it

1 requires an additional set of I/O pins for the chip so that the
2 external debug memory can be coupled to the chip. This may
3 require a significant number of pins since the addresses to be
4 mapped may be 32 or 64 bits wide.

5
6 Still another tracing and trapping method is disclosed in
7 U.S. Patent Number 5,513,346 to Satagopan et al. entitled "Error
8 Condition Detector for Handling Interrupt in Integrated Circuits
9 Having Multiple Processors." According to this method, an
10 interrupt processor controller intercepts all interrupts and
11 routes them to the appropriate processor in a multiprocessor chip.
12 The interrupt processor controller includes logic which determines
13 when an interrupt will cause an error because a previously
14 instigated interrupt has not been cleared. When such an error is
15 detected, a bit is set in an error detect register, the bit
16 corresponding to an interprocessor interrupt channel. The bits in
17 the register are ORed and a single bit output indicates the
18 occurrence of an error. The register may then be examined to
19 determine the location of the interrupt error in the executing
20 code. This method does not interfere with the system bus and does
21 not require very many additional pins on the chip. However, the
22 debugging information that it provides is limited.

1 The Motorola MPC-860 PowerQuicc™ includes a program
2 development system interface port which provides a three bit
3 output indicative of the state of the program execution as the
4 program is being executed. The MPC-860 is a 40 mHz communications
5 controller but the development system interface port is only
6 operable at a rate of 4 mHz. Thus, the port can not be used for
7 real time debugging. The specifications for the MPC-860 are found
8 in the "MPC-860 POWERQUICC USER'S MANUAL", Copyright 1996 .
9 Motorola, Inc., Schaumburg, IL, the complete disclosure of which
10 is incorporated herein by reference.

11
12 ASIC design using one or more embedded processors poses
13 additional debugging challenges. The prior art methods of
14 trapping instructions at a given point in time implies that the
15 system must be stopped to allow debugging of firmware. Once the
16 system is stopped, however, real time events and their timing
17 relationships are lost. If there is a firmware bug which is only
18 identifiable in the presence of live traffic (during real time
19 operations) it is necessary to obtain contextual information about
20 the error before the firmware is changed.

1 SUMMARY OF THE INVENTION

2
3 It is therefore an object of the invention to provide a
4 debugging interface for tracing instructions without loss of real
5 time context and event interaction.
6

7 It is also an object of the invention to provide a debugging
8 interface which does not interfere with the operation of a
9 processor or system bus.

10
11 It is another object of the invention to provide a debugging
12 interface which does not require many additional pins on a
13 processor chip.
14

15 It is a further object of the invention to provide a
16 debugging interface which provides access to a substantial amount
17 of information about the executed instructions.
18

19 In accord with these objects which will be discussed in
20 detail below, the debugging interface of the present invention
21 includes a first decoder coupled to the sequencer of a processor
22 and to the Instruction RAM (IRAM) of the processor. The first
23 decoder, according to the invention, provides a real time three
24 bit output on a cycle by cycle basis which is indicative of the

1 processor activity during the last clock cycle. According to a
2 presently preferred embodiment, the three bit output indicates
3 seven different conditions regarding processor activity. In
4 particular, the three bit output indicates whether or not a new
5 instruction has been executed since the last clock cycle, and if a
6 new instruction has been executed, whether the last instruction
7 executed by the processor was an immediate jump, a jump to
8 register, or a branch taken. In addition, the three bit output
9 will indicate whether execution of the instruction resulted in an
10 exception. By recording this three bit output over time, and
11 comparing it to the actual instructions listed in the program
12 code, important debugging information is obtained about a program
13 which was running in real time.

14
15 According to a preferred embodiment of the invention, a
16 second decoder and an event history buffer are coupled to the
17 cause register of the sequencer of the processor. In particular,
18 the second decoder is coupled to the enable input of the history
19 buffer and the cause register is coupled to the data input of the
20 history buffer. The second decoder decodes the contents of the
21 cause register and enables the history buffer whenever the
22 contents of the cause register indicates an exception, a jump
23 register instruction, or a change in the status of an interrupt
24 line. Whenever the history buffer is enabled, information from

1 the cause register and the program counter is loaded into the
2 buffer. By recording the contents of the history buffer over
3 time, and comparing the information to the actual program code,
4 additional important debugging information is obtained about a
5 program which was running in real time. According to this
6 preferred embodiment of the invention, the seventh condition
7 indicated by the three bit output of the first decoder is whether
8 an exception was encountered without writing to the history
9 buffer.

10
11 According to the presently preferred embodiment, each entry
12 in the event history buffer is forty-four bits. Each forty-four
13 bit entry in the history buffer includes the current sixteen bit
14 time stamp, twenty three bits from certain fields of the cause
15 register or program counter, one bit indicating whether the entry
16 is related to a jump or an exception, two bits identifying the
17 processor number (in a multiprocessor system), one bit identifying
18 whether the history buffer has overflowed, and a time stamp
19 rollover bit. The history buffer preferably has a depth of at
20 least sixteen entries.

21
22 An exemplary implementation of the debugging interface is
23 embodied on an ASIC chip having three processors. Each processor
24 is provided with two decoders as described above and a single

1 event history buffer is provided on the chip. Nine pins on the
2 chip are used to provide access to the three bit outputs of each
3 first decoder. Three pins on the chip provide serial access
4 (data, clock, and enable) to the contents of the event history
5 buffer. These twelve pins on the chip allow a diagnostic device
6 to be coupled to the chip during real time operations without
7 interfering with the operation of the chip. The outputs of the
8 first decoders and the contents of the event history buffer can be
9 recorded over time by the diagnostic device to provide a real time
10 record of the processing events occurring in the chip during real
11 time. This real time record taken together with knowledge of the
12 program code being executed provides a true picture of the
13 processors' execution sequence in real time and thereby expedite
14 debugging of code.

15
16 Additional objects and advantages of the invention will
17 become apparent to those skilled in the art upon reference to the
18 detailed description taken in conjunction with the provided
19 figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 (represented as Figs. 1A and 1B on two separate sheets) is a schematic block diagram of an exemplary implementation of a real time debugger interface according to the invention; and

Figure 2 is a schematic block diagram of a debugging system coupled to a chip embodying a real time debugger interface according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Figures 1, an exemplary ASIC chip 10 incorporating a debugger interface according to the invention includes three processors 12a, 12b, 12c, sharing a common clock 16 via a clock bus 17. Each processor includes an instruction RAM (IRAM) 18a, 18b, 18c, an arithmetic logic unit (ALU) 20a, 20b, 20c, and a "sequencer" 22a, 22b, 22c. Each sequencer includes a program counter 24a, 24b, 24c and a cause register 26a, 26b, 26c. Each program counter contains an index of the instructions in an associated IRAM and a pointer to the index as the instructions are executed by the processor. The cause registers store current information about interrupts, exceptions, and other processor functions.

1 According to one aspect of the invention, a first decoder
2 28a, 28b, 28c is coupled to each IRAM 18a, 18b, 18c, and to each
3 sequencer 22a, 22b, 22c, i.e., to each program counter and each
4 cause register. Each first decoder has a three bit output 30a,
5 30b, 30c which is available off the chip 10 via three pins (0, 1,
6 2) in real time.

7
8 As mentioned above, the three bit output of each first
9 decoder 28 provides an indication of the processor activity during
10 the last clock cycle. Thus, the decoder 28 is arranged to
11 indicate whether the program counter has moved its pointer to a
12 new instruction. The decoder also decodes the instruction in the
13 IRAM to provide information about the instruction, and decodes the
14 contents of the cause register to provide an indication of an
15 exception encountered during the execution of an instruction.
16 According to a presently preferred embodiment, the first decoder
17 28 generates a three bit output which is interpreted as shown in
18 Table 1, below.

Output	Mnemonic	Description
000	NC	No Change
001	INC	Program Counter Increment
010	JI	Program Counter Jump Immediate
011	JR	Program Counter Jump Register
100	ECP	Exception Encountered
101	PBT	Program Counter Branch Taken
110	RSD	Reserved
111	ENH	Exception Encountered, No History Buffer Entry Written

Table 1

The output 000 indicates that there has been no change in the processor since the last clock cycle; i.e., the processor has not processed a new instruction and the program counter pointer has not changed. The output 001 indicates that the processor has processed the next instruction in the program; i.e., the program counter pointer has incremented to the next instruction in the index. The output 010 indicates that the last instruction processed by the processor was a "hard coded" jump to an instruction; i.e., the instruction in IRAM pointed to by the

1 program counter includes code indicating that it is a jump
2 instruction to an absolute address in the program. The output 011
3 indicates that the last instruction processed by the processor was
4 a jump to an instruction based on the contents of a register;
5 i.e., the instruction in IRAM pointed to by the program counter
6 includes code indicating that it is a jump instruction to a
7 location in the program determined by the value of a variable.
8 The output 100 indicates that since the last clock cycle the
9 processor has encountered an interrupt or an exception; i.e., the
10 contents of the cause register contain code which indicates an
11 interrupt or exception. The output 101 indicates that the last
12 instruction processed by the processor was a pc branch taken;
13 i.e., the instruction in IRAM pointed to by the program counter
14 includes code indicating that it is a branch back to another
15 instruction. The output 110 is not presently used, but is
16 reserved for future use. The output 111 indicates that since the
17 last clock cycle the processor has encountered an interrupt or an
18 exception; and that no entry was made in the history buffer

19
20 The operation of the first decoder 28 and its output is
21 illustrated with reference to a simple code listing which is shown
22 below in Table 2.

23

LINE NUMBER	INSTRUCTION
10	Input A
20	B=5
30	C=2
40	D=B+C
50	If D=7 then Goto 70
60	Goto A*10
70	B=4
80	Goto 30
90	End

Table 2

The listing in Table 2 has one "immediate" or "hard coded" jump instruction at line 80 and a conditional branch at line 50. It also has one jump instruction, line 60, based on the contents of a register, i.e. the value of A which is input at line 10. The three bit output of the first decoder during execution of the instructions shown in Table 2 is illustrated in Table 3 below where the values of variables A, B, C, and D are also shown.

Current Line	Next Line	A	B	C	D	Mnemonic	Three Bit Output
10	20	?	?	?	?	INC	001
20	30	?	5	?	?	INC	001
30	40	?	5	2	?	INC	001
40	50	?	5	2	7	INC	001
50	70	?	5	2	7	PBT	101
70	80	?	4	2	7	INC	101
80	30	?	4	2	7	JI	010
30	40	?	4	2	7	INC	001
40	50	?	4	2	6	INC	001
50	60	?	4	2	6	INC	001
60	?	?	4	2	6	JR	011

Table 3

When the first instruction (listed in line 10) is executed, the first decoder indicates that a program counter increment (INC) in the execution of the program has occurred and shows an output of "001". As the program progresses from the instruction on line 10 through the instruction on line 40, the first decoder continues to indicate that a program counter increment (INC) in the execution of the program has occurred and continues to show an output of "001". When the instruction on line 50 is executed, the first decoder indicates that a program counter branch taken (PBT)

1 has occurred and shows an output of "101". As seen in Tables 2
2 and 3, the program branches to line 70 because the conditional
3 expression of line 50 is true based on the variable D=7. Upon
4 execution of line 70, the first decoder indicates that a program
5 counter increment (INC) in the execution of the program has
6 occurred and shows an output of "001". When the instruction on
7 line 80 is executed, the first decoder indicates that an immediate
8 jump (JI) has occurred and shows an output of "010". As seen in
9 Tables 2 and 3, the program jumps to line 30. When the
10 instructions on lines 30 and 40 are executed, the first decoder
11 indicates that a program counter increment (INC) in the execution
12 of the program has occurred and shows an output of "001". When
13 line 50 is executed (now for the second time) the first decoder
14 indicates that a program counter increment (INC) in the execution
15 of the program has occurred and shows an output of "001" because
16 the condition (D=7) for the jump in line 50 is no longer valid.
17 Line 60 is now executed and a jump to a location stored in a
18 register occurs. The first decoder therefore indicates a jump to
19 register (JR) by showing an output of "011".

20
21 Referring once again to Figure 1, according to another aspect
22 of the invention, each cause register 26a, 26b, 26c is coupled to
23 the data input D of an event history buffer 14 and a second
24 decoder 32a, 32b, 32c is coupled to each cause register and to the

1 enable input E of the history buffer 14. The clock 16 provides
2 the common clock signal to the clock input C of the history buffer
3 14 via the clock bus 17, and a timestamp register 19 is also
4 coupled to the clock bus 17. The contents of the history buffer
5 14 are made available off chip by three pins for the data, clock,
6 and enable (D, C, E) of the history buffer 14. According to this
7 aspect of the invention, when certain conditions are detected by
8 one of the second decoders 32, the history buffer is enabled via
9 the appropriate decoder, and information from the cause register,
10 the timestamp register, and the program counter is stored in the
11 history buffer. More particularly, the second decoder 32 enables
12 the history buffer whenever the first decoder contains code which
13 indicates that the processor is processing an instruction to jump
14 to a location stored in a register, whenever the first decoder
15 contains code indicating an exception was encountered, and
16 whenever the first decoder contains code indicating a change in
17 state of an interrupt line.

18
19 According to a presently preferred embodiment, when the
20 history buffer is enabled, it captures forty-four bits of
21 information from the cause register or program counter, and the
22 timestamp register. The forty-four bits of information are
23 preferably organized as illustrated in Table 4 below.

43	42	41	40 - 18	17	16	15 - 0
Mode	Proc	Cause/PC	HOVRF	TR	Time Stamp	

Table 4

The first bit, bit location 43, is a mode identifier indicating whether the entry being stored has program counter information or cause register information. A two bit processor identification number is stored in binary form at bit locations 42, 41. This number is used to indicate which processor's information is being stored (in the case of a multiprocessor system). The next twenty-three bits at bit locations 40 through 18 are used to store cause register information or program counter information depending on the mode as explained above. If program counter information is being stored, the contents of the program counter are stored at bit locations 40 through 18. If cause register information is being stored, bit location 40 is used to indicate whether the exception occurred while the processor was executing an instruction in the branch delay slot. (This applies to pipelined processors such as RISC processors.) Bit locations 39 through 35 are used to store processor related exception conditions. Bit locations 34 through 18 are used to store an indication of all pending interrupts (external, software, co-processor). The HOVRF field at bit location 17 is used to indicate

1 whether the internal event history buffer has overflowed. The TR
2 bit 16 is used to indicate a timestamp rollover and bits 15
3 through 0 are used to store a sixteen bit timestamp. According to
4 the presently preferred embodiment, the forty-four bits captured
5 in the history buffer 14 are serially output on data pin D over
6 forty-four clock cycles (bit serial output).

7
8 As mentioned above, the event history buffer records
9 information when an event (either an unmasked exception or a PC
10 jump register instruction) has occurred. According to a presently
11 preferred embodiment, this requires an additional mask register
12 per cause register and a free running timestamp counter. The
13 event masks are provided by a JTAG test register load instruction
14 in the static debug interface. When the cause register bits
15 corresponding to an exception are unmasked or a PC jump register
16 instruction is encountered, an entry is made in the history
17 buffer.

18
19 Those skilled in the art will appreciate that the outputs of
20 the first decoder 28 and the contents of the history buffer 14
21 provide a relatively complete indication of each processor's
22 execution sequence in real time, particularly when viewed in light
23 of the actual program code which is being executed. Therefore,

1 according to the invention, a debugging system may be coupled to
2 the first decoders and history buffer as illustrated in Figure 2.
3

4 Turning now to Figure 2, the outputs 30a, 30b, 30c of the
5 first decoders and the D,C,E terminals of the history buffer are
6 coupled to a debugging computer 44 which preferably has a copy of
7 the program code stored therein. The three-bit outputs 30a,30b,
8 30c of the first decoders and the D,C,E terminals of the history
9 buffer are preferably coupled to an interface buffer 40 which is
10 coupled by a serial, parallel, or network connection 42 to the
11 debugging computer 44. The interface buffer 40 is a rate
12 decoupling buffer. In a present embodiment of the invention, the
13 debugger interface is provided on a 100 MHz three processor
14 system. In that system, the data rate for reading the event
15 history buffer is approximately 1 gigabit/sec. Current PCs cannot
16 keep up with that data rate. Therefore, the buffer 40 is provided
17 to prevent the loss of event history data.
18

19 As the program is running on the ASIC 10, the debugging
20 computer 44 collects information from the first decoders and the
21 history buffer. The information collected by the computer 44 is
22 associated with each line of code being executed by the ASIC by
23 stepping through the copy of the code which is stored in the
24 computer 44. When a bug is encountered, the complete history of

1 instruction execution leading up to the failure can be reviewed
2 with the computer 44. The debugging system is non-invasive and
3 permits debugging of programs operating in real time.
4

5 There have been described and illustrated herein embodiments
6 of a real time debugger interface for embedded systems. While
7 particular embodiments of the invention have been described, it is
8 not intended that the invention be limited thereto, as it is
9 intended that the invention be as broad in scope as the art will
10 allow and that the specification be read likewise. Thus, while
11 particular encoding schemes have been disclosed with reference to
12 the first decoder output and the history buffer contents, it will
13 be appreciated that other encoding schemes could be utilized
14 provided that they achieve substantially the same results as
15 described herein. Also, while the invention has been illustrated
16 with reference to a three-processor ASIC chip, it will be
17 recognized that the invention may be applied in other types of
18 chips having greater or fewer processors. Moreover, while
19 particular configurations have been disclosed in reference to the
20 indications provided by the first decoders, it will be appreciated
21 that other configurations could be used as well, provided that
22 they achieve substantially the same results as described herein.
23 It will therefore be appreciated by those skilled in the art that

- 1 yet other modifications could be made to the provided invention
- 2 without deviating from its spirit and scope as so claimed.